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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/877,792	SANCHEZ ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response on 7 February 2006 has added claims 41 and 42. Claims 1-6 and 9-42 are pending in this application.

Claims 1-6 and 9-42 have been rejected.

Claim Rejections – 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-6, and 9-42 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 37 recite a limitation of "providing a circuit simulator having the capability of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature" (emphasis added) which renders the claim indefinite. It is unclear from the language of the claim whether the recited features are performed as components of the method. It is unclear how the recited functions contribute to the claimed method.

Claim 1 recites a method that is functionally equivalent to:

> A method for making an integrated circuit, comprising:

Providing a first circuit design;

Changing the first circuit design to obtain a second circuit design; and

Making an integrated circuit comprising the second circuit design.

None of the other recited steps contribute to the stated purpose of the preamble. The steps of "providing a circuit simulator", "providing an equation", "applying the circuit simulator to the first circuit design", "replacing the unknown constants", and "performing a first set of timing analyses" are unrelated to the result of the method, specifically the "integrated circuit comprising the second circuit design". The language of claim 1 fails to particularly point out and distinctly claim the invention by reciting several steps that do not contribute to the method.

Similarly, Claim 37 recites a method that is functionally equivalent to:

A method for obtaining a performance model, comprising:

Providing a path comprising a first design block, a second design block, and an interconnect coupling the first design block to the second design block;

Changing the design of at least one of the interconnect, the first design block, and the second design block to obtain a revised path; and

Making an integrated circuit comprising the revised path.

The language of claim 37 fails to particularly point out and distinctly claim the invention by reciting several steps that do not contribute to the method.

Claim 2 recites additional steps of claim 1, apparently to be performed after the completion of the method of claim 1, however claim 1 has achieved the stated purpose of the preamble. In that circumstance, the steps of claim 2 would fail to contribute to the method, which has been fulfilled by claim 1, and these steps would be, at best, optional. Claim 2 is vague and indefinite for at least the ambiguity regarding the sequence of steps and whether the steps of claim 2 contribute to the method.

Claim 3 recites the limitation "wherein the plurality of variables are related to power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature," however the relation defined by these claims is undefined. Recitation of the term "related" is so broad that the only interpretation excluded from this language would be "unrelated" or "not related". One reasonable interpretation of the claim would rely on the observation that all of power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature are inherently related to each other in the field of integrated circuits, as would be recognized by a person of ordinary skill in the art, and therefore the claim would be anticipated by a variable "related to an integrated circuit". Recognizing that integrated circuit model numbers commonly denote operating temperatures or required power supply voltages, it is unclear what is properly excluded from the language of this claim. The language fails to particularly point out and distinctly claim the invention.

Regarding claims 4, 13, and 25, the independent claim 1 which is directed to a method, recites steps of "providing an equation", "replacing the unknown constants [...] to obtain a

performance model", and "performing a first set of timing analyses using the performance model". While these steps are not indefinite per se, they broadly define an abstract method. For example, the claim contains no positive recitation of how to "provide an equation", what is literally involved in "obtaining a performance model", what type of timing analyses are performed, or how the timing analyses use the performance model. These recitations in claim 1 may not be improper under 35 U.S.C. § 112, however they create difficulties regarding claims 4, 13, and 25.

Dependent claims 4, 13, and 25 attempt to recite further limitations in the form of additional structure of the equation. These claims do not further limit the method of claim 1. Because claim 1 vaguely and broadly recites the use of the equation, the additional structure recited in claims 4, 13, and 25 have no direct relation to the method steps of claim 1. The inclusion of, for example "delay expressions" in the equation of claim 1 does nothing to limit the method defined by claim 1 because there exists no positive recitation in claim 1 of how the method depends upon, uses, manipulates, or recognizes "delay expressions" in the equation. Therefore, the method of claim 4 is functionally equivalent to the method of claim 1, and similarly claims 13 and 25.

The metes and bounds of claims 4, 13, and 25, as intended by the claim language, are indefinite. It is unclear how these limitations further define the method of claim 1.

Dependent claims 5-12, 14-24, 26-35, and 40 stand rejected by virtue of their dependence and for the reasons stated above regarding claims 4, 13, and 25. The Examiner respectfully suggests that Applicants define a claimed method in terms of the steps performed rather than the structure of the components used in the method.

Claims 41-42 stand rejected by virtue of their dependence.

Claim 36 recites a limitation wherein "one of the variables is related to at least one of metallization capacitance and metallization resistance" however the relation defined by these claims is undefined. Claim 36 is rejected for the same reasons given above regarding claim 3.

Claims 38-39 recite limitations "wherein the plurality of variables are further related to metallization capacitance and metallization resistance" and "wherein the plurality of variables are further related to capacitive load" however the relation defined by these claims is undefined. Claims 38-39 are rejected for the same reasons given above regarding claim 3.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Response to Arguments – 35 USC § 112, second paragraph

In response to the rejections set forth above, Applicants argue that:

> The Examiner states that because claims 1 and 37 recites a limitation of "providing a circuit simulator having the capability of simulating changes to at least one of power supply voltage, ...", the claims are indefinite. Applicants respectfully disagree. Firstly, this element is simply defining what type of circuit simulator is to be applied to the first circuit design to derive the first set of constants for the plurality of constants. That is, the circuit simulator should be capable of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature. Secondly, the claim clearly includes how this circuit simulator is used (e.g. "applying the circuit simulator to the first circuit design...") Therefore, this language is clear and definite.

The Examiner respectfully traverses this argument as follows.

The phrase "providing a circuit simulator having the capability of simulating changes ..." is vague and indefinite because this language does not positively define what type of circuit

simulator is to be applied. It is impossible to conduct a proper examination of this claim language because it would be impossible to look to the prior art and determine what circuit simulators are covered by this language. Indeed a circuit simulator that is explicitly described as having this functionality is covered by this language. However this is not what the claim requires. It is perfectly reasonable that a circuit simulator touted as having some other feature **is capable of simulating the recited changes** however this fact must be transcended from some obscure source of knowledge. Of course, the capabilities of a prior art simulator may depend not on the simulator itself but rather how it is used by one skilled in the art. Thus a simulator which, under most circumstances is not encompassed by this language, indeed has the capability to of simulating the recited changes when used by an artisan of ordinary skill with a little creativity.

This claim language does not define the circuit simulator. This claim language, were it definite within the meaning of 35 U.S.C. § 112, second paragraph, would require the Examiner to identify the undisclosed, undocumented, or perhaps previously unknown **latent capabilities** of prior art simulators as used by skilled artisans. Applicants' arguments on this point have been fully considered but have been found unpersuasive.

Applicants further argue that:

> The elements stated in claim 1 are clearly related to the result of "making an integrated circuit comprising the second circuit design." That is, as recited in claim 1, an equation must be provided, a first set of constants derived, using the first set of constants to obtain a performance model, and performing a first set of timing analyses using the performance model of the first circuit design. These steps are required with respect to the first circuit design, and clearly contribute to the claimed method. Simply because the first design can be changed to a second circuit design which is included in the integrated circuit does not mean that any steps related to the first circuit design do not contribute to the overall method.

The Examiner respectfully traverses this argument as follows.

Applicants' argument mischaracterizes the claim as written. Applicants' statement that "Simply because the first design **can be changed** to a second circuit design" disregards that the claim positively recites and requires "**changing the first circuit design to obtain a second circuit design.**" There are no additional limitations placed upon the "second circuit design" except it is unambiguously clear from the claim language that the second circuit design is "changed," i.e. different from and not equivalent to the first circuit design. The steps of providing an equation, applying the circuit simulator, deriving constants, and performing a first set of timing analyses apply to **the first circuit design which is different from and not equivalent to the second circuit design**.

How do any of these steps as applied to the first circuit design have any role in the formation of the second circuit design? One could perform innumerable tests to the first circuit design and have absolutely no impact whatsoever on the second circuit design. To reiterate, the claim places no limitation on the second circuit design except that it is achieved by changing the first circuit design. The Examiner maintains that the above-identified steps of claim 1 are unrelated to the result of the method and therefore do not define the method. Applicants' arguments on this point have been fully considered but have been found unpersuasive.

Applicants further argue that:

> With respect to claim 2, Applicants agree with Examiner that claim 2 recites additional steps of claim 1 and that these steps would be optional. That is, any dependent claim can be considered as "optional" since they add optional elements to the independent claim. The Examiner states that "claim 1 has achieved the stated purpose of the preamble" and that therefore "the steps of claim 2 would fail to contribute to the method, which has been fulfilled by claim 1, and these steps would be, at best, optional." The Examiner, for this reason, states that claim 2 is vague and indefinite. However, under the Examiner's logic, any dependent claim in any existing patent would be invalidated. Furthermore, the Examiner indicates that the steps of claim 2 are "apparently to be performed after the completion of claim 1." However, not that these steps appearing in a dependent claim do not imply order, and may be performed anywhere within the method of claim 1 and do not necessarily have to be performed after completion of claim 1.

The Examiner respectfully traverses this argument as follows.

To directly refute Applicants' allegation, the Examiner's logic does not support that "any dependent claim in any existing patent would be invalidated." To the contrary, the Examiner merely suggests that improper dependent claims that fail to further limit the parent claim do not comply with 35 U.S.C. § 112. The Examiner does not understand 35 U.S.C. § 112, fourth paragraph, as creating provisions for "optional limitations." The Examiner understands proper dependent claims to "specify a further limitation of the subject matter claimed".

In the present application, claim 2 recites steps that are, from all appearances as well as Applicants' arguments, optional.

Further, the Examiner respectfully suggests that Applicants carefully consider whether claim 2 complies with 35 U.S.C. § 112, second paragraph, where "these steps appearing in a dependent claim do not imply order, and may be performed anywhere within the method of claim 1 and do not necessarily have to be performed after completion of claim 1." Claim 2 clearly recites, *inter alia*, "applying a circuit simulator to the second circuit design..." which plainly implies an order to the steps. The "second circuit design" does not exist until it is created in the step of "changing". Alternatively, an additional ground of rejection under 35 U.S.C. § 112, second paragraph, may be necessary. If Applicants' argument means that the steps recited by claim 2 may be performed between the steps of "changing" and "making" in claim 1, it remains unclear why Applicants would insist that these steps "may be performed anywhere within the method of claim 1," which argument substantiates the conclusion that these claims are indefinite.

Applicants' arguments on this point have been fully considered but have been found unpersuasive.

Applicants further argue that:

> With respect to claim 3, the Examiner states that recitation of the term "related" is so broad that "it is unclear what is properly excluded from the language of this claim" and proceeds to conclude that "the language fails to particularly point out and distinctly claim the invention." However, even though the term "related" can be broadly interpreted, it does not make the claim indefinite under 35 U.S.C. § 112. Furthermore, the metes and bounds of what is being claimed is clear, where the variables of the equations are described through the specification, such as throughout pages 6-21. Furthermore, there can be other aspects of an integrated circuit not related to the parameters provided in claim 3; therefore, the Examiner cannot simply say that the claim would be anticipated by any variable "related to an integrated circuit." At a minimum, the variables have to be related to power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature. Therefore, although the language of claim 3 may be broad, Applicants submit that claim 3 is still definite and therefore patentable under 35 U.S.C. § 112.

The Examiner respectfully traverses this argument as follows.

Applicants are respectfully reminded that it is the claim, not the specification, which defines the claimed invention. The claim does not incorporate the teachings of pages 6-21 of the specification. Rather, the claim ambiguously recites that the variables are "related". Applicants submit that "there can be other aspects of an integrated circuit not related to [power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature]" but provide no examples or further explanation. Of course, the meaning of the term "related" is completely open to interpretation and debate, and the list of parameters already encompasses basically all relevant parameters of an integrated circuit. The Examiner reiterates that it is unclear what is properly excluded from the language of this claim.

At the risk of being absurd, the integrated circuit's elevation above sea level would be related to the atmospheric pressure, relative wind speed, and temperature. The number of components present in the integrated circuit place would be related to the load placed on the

power supply voltage. The insulating substrate creates the capacitive effect between conductors in the integrated circuit and is thus related to the metallization capacitance. There is no end to this exercise. There is no suggestion in this application that any of these interpretations are unreasonable. Claim 3 apparently presents no reasonable limitation on the invention whatsoever.

Applicants' arguments on this point have been fully considered but have been found unpersuasive.

Applicants further argue that:

> The Examiner, with respect to claim 4, 13, and 25, state that these claims "do not further limit the method of claim 1." The Examiner proceeds to state that "because claim 1 vaguely and broadly recites the use of the equation, the additional structure recited in claims 4, 13, and 25 have no direct relation to the method steps of claim 1." However, Applicants respectfully disagree. Each of these claims further limits the method of claim 1 by further defining the equation which is applied. The Examiner states that "the inclusion of, for example, 'delay expressions' in the equation of claim 1 does nothing to limit the method defined by claim 1 because there exists no positive recitation in claim 1 of how the method depends upon, uses, manipulates, or recognizes 'delay expressions' in the equation." Applicants disagree. Firstly, the equation is clearly used in claim 1, where the equation, in the embodiment of dependent claim 4, has to further include a delay expression.

The Examiner respectfully traverses this argument as follows.

Applicants' argument attempts to distinguish the method of claim 1 from the method of claims 4, 13, and 25 based strictly upon the contents of the equation. As stated previously, claim 1 presents no positive recitation of how the method depends upon, uses, manipulates, or recognizes 'delay expressions' or any other expressions. Therefore, it is entirely irrelevant to the method of claim 1 what expressions the equation comprises. The claimed invention contains no description whatsoever of the role these "expressions" play in the equation. There exists no link in the claimed invention between the "expressions" of claims 4, 13, and 25 and the method steps of claim 1.

Applicants state, "the equation is clearly used in claim 1." The Examiner does not understand Applicants' argument. Claim 1 recites a step of "providing an equation which comprises a plurality of variables and constants, wherein the plurality of constants are unknown constants and one of the variables is related to at least one of metallization capacitance and metallization resistance." **There is no further recitation of an "equation" or its "use" anywhere in claim 1.** Nowhere in claim 1 is a "result" of this equation "clearly used".

Nevertheless, claim 1 contains no consideration whatsoever for any of the "expressions" in the equation. We might imagine that the equation comprises any conceivable expressions, both narrowly interpreted and broadly, reasonable and absurd. **None of these expressions play any role in the positively recited steps and therefore fail to define the method of claim 1.**

If Applicants believe the Examiner's conclusion to be in error, the Examiner respectfully requests that Applicants kindly furnish the Examiner with support from the MPEP or law that would substantiate the argument that a proper dependent claim may further limit a structure which is either entirely absent from or completely irrelevant to the method of a parent claim.

Applicants' arguments on this point have been fully considered but have been found unpersuasive.

Applicants further argue that:

> Also, the method of claim 4 is not functionally equivalent to the method of claim 1, as asserted by the Examiner, because in claim 1, the equation that is provided and used within the method need not include the delay expressions of claim 4.

The Examiner respectfully traverses this argument as follows.

This issue has been addressed above. To further clarify, the Examiner asserts that claim 4 is **functionally** equivalent to claim 1. Applicants have yet to show how the inclusion of "delay expressions" changes the **function** of claim 1 in any way.

Applicants' arguments on this point have been fully considered but have been found unpersuasive.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-6 and 9-42 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The numerous difficulties under 35 U.S.C. § 112, second paragraph, set forth above, necessitate this rejection of the claims under 35 U.S.C. § 112, first paragraph. The claims as drafted are drawn to an invention that is not disclosed in the specification. The method defined by the explicitly recited claim language of claims 1 and 37, as explained above, fails to require several critical steps. Specifically, the disclosed inventive method is not required by the method

defined in these claims. Applicants are respectfully encouraged to draft claims that are limited to the disclosed invention.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Response to Arguments – 35 USC § 112, first paragraph

In response to the rejections set forth above, Applicants argue that:

> For example, each of the delay, capacitance and setup/hold time equations are fully described in pages 6-21, and a method of using these equations to make an integrated circuit is described on pages 21-27, with respect to, e.g., FIG. 8. This text clearly supports each of these claims. Therefore, the claims are clearly patentable under 35 U.S.C. § 112.

The Examiner respectfully traverses this argument as follows.

Applicants' argument makes reference to pages 6-27 of a 28 page specification, omitting almost nothing except the description of the prior art and the brief description of the drawings. Applicants' arguments are conclusory statements that do not overcome the rejections of record.

Applicants further argue that:

> The Examiner states that "the numerous difficulties under 35 U.S.C. § 112, second paragraph, set forth above, necessitate this rejection of the claims under 35 U.S.C. § 112, first paragraph." As pointed out in the above discussions, Applicants submit that there are no difficulties present under 35 U.S.C. § 112, second paragraph. The Examiner further states that "the claims as drafted are drawn to an invention that is not disclosed in the specification." However, this is incorrect. The claims are clearly described throughout the specification.

The Examiner respectfully traverses this argument as follows.

The rejections under 35 U.S.C. § 112, second paragraph, still present in this application, have been addressed above.

Regarding the description of the claimed invention, the Examiner respectfully draws Applicants' attention to the plain and unambiguous language of claim 1 which merely requires:

A method for making an integrated circuit, comprising:

Providing a first circuit design;

Changing the first circuit design to obtain a second circuit design; and

Making an integrated circuit comprising the second circuit design.

As explained above, the other recited steps are irrelevant to the invention as claimed. If Applicants feel that this method is adequately described by the specification, the Examiner respectfully requests that Applicants provide specific citation of the portions of the specification that support this 3 step method and the Examiner will properly reconsider the propriety of this rejection. However, the Examiner has determined that this 3 step method cannot properly be regarded as the subject of Applicants' disclosure and has therefore entered this rejection in an attempt to illustrate the significant disconnect between the disclosed invention and the claimed invention.

Applicants' arguments on this point have been fully considered but have been found unpersuasive.

Applicants' response is essentially directed toward the disclosed invention and not to the claimed invention. The Examiner has exerted significant effort to illustrate the shortcomings of the claim language. The Examiner respectfully suggests that Applicants carefully consider the meaning of the claim language under 35 U.S.C. § 112 to determine if it appropriately represents the disclosed invention. MPEP 2106 (II) (C) states:

> The claims define the property rights provided by a patent, and thus require careful scrutiny. The goal of claim analysis is to identify the boundaries of the protection sought by the applicant and to understand how the claims relate to and define what the applicant has indicated is the invention. Office personnel must first determine the scope of a claim by thoroughly analyzing the language of the claim before determining if the claim complies with each statutory requirement for patentability.

The Examiner respectfully suggests that careful attention be paid to the claim language in order to expedite prosecution and to facilitate a proper analysis of any novelty or non-obviousness that may be present in the claimed invention.

Claim Interpretation

Because of the 35 U.S.C. § 112, first and second paragraph rejections, the claims are so indefinite and incomplete that no art rejection would be warranted, as substantial guesswork would be involved in determining the scope and content of these claims. It is essentially unknown what the metes and bounds of the claims are or where Applicants intend for those metes and bounds to lie. See *In re Steele,* 305 F.2d 859, 134 USPQ 292 (CCPA 1962); *Ex parte Brummer,* 12 USPQ 2d, page 1654; and also *In re Wilson,* 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). However, in the interest of compact prosecution, an art rejection will be asserted in view of the broadest and most reasonable interpretation of the claims. *Ex parte Ionescu,* 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

The claims are interpreted **specifically according to the plain and unambiguous language of the claim as:**

1. A method for making an integrated circuit, comprising:

Providing a first circuit design;

Changing the first circuit design to obtain a second circuit design; and

Making an integrated circuit comprising the second circuit design.

37. A method for obtaining a performance model, comprising:

Providing a path comprising a first design block, a second design block, and an interconnect coupling the first design block to the second design block;

Changing the design of at least one of the interconnect, the first design block, and the second design block to obtain a revised path; and

Making an integrated circuit comprising the revised path.

The claim language is drafted in such a way that the remaining text of the claims is superfluous and fails to contribute in any meaningful way to the claimed method.

Response to Arguments – Claim Interpretation

Applicants submit that:

> The drafted claims are all definite and clearly supported by the Specification. And although the Examiner may assert an art rejection in view of the broadest and most reasonable interpretation of the claims, the Examiner still has to be reasonable in his interpretation and address all claim elements.

The Examiner disagrees that the claims are definite and clearly supported by the specification as per the rejections and response above, however agrees with the remainder of Applicants' statement.

Applicants further submit:

> Secondly, Applicants wish to point out that the pertinence of the cited prior art reference with respect to the rejection of the independent claims and their respective dependent claims is not apparent and, further, that the rejection of the claims is not clearly explained as pert he requirements outlined in 37 C.F.R. 1.104(c)(2). Applicants also respectfully points out to the Examiner that "[a] plurality of claims should never be grouped together in a common rejection, unless the rejection is equally applicable to all claims in the group" (MPEP 707.07(d)). In the current rejection, the Examiner does not address each and every claim element of claim 1 and 37, and does not address any of the dependent claims, which all include elements which differ from those of the independent claims.

The Examiner's response is as follows.

> 37 CFR 1.104(c)(2), as relied upon by Applicants, states:
>
> > In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, **the particular part relied on must be designated as nearly as practicable**. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified. (emphasis added)

The claim language in this application is significantly disconnected from the disclosure. The claim language contains numerous ineffective method steps which have ultimately no bearing whatsoever on the result of the claimed method. The Examiner has applied the prior art **as specifically as practicable** in light of the claim language.

The Examiner is unable to respond in any more detail to Applicants' statement that the pertinence of the prior art rejection is not apparent. The Examiner respectfully encourages Applicants to carefully review the claim language and to consider whether it properly corresponds to what Applicants have invented.

The Examiner has addressed each and every claim element of claims 1 and 37 which contribute to the conclusion of the method. Applicants' claim language renders numerous steps optional at best and therefore superfluous when looking to the prior art for **anticipatory and equivalent teachings**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

3. Claims 1-6 and 9-42 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,018,623 to Chang et al. (Chang).

Chang teaches the influence of metallization resistance and metallization capacitance on integrated circuit performance and the importance of estimating (simulating) these effects during integrated circuit design [*"Variations in interconnect resistance ® and capacitance © create variances in the circuit delay and crosstalk. If the circuit delay or interconnect crosstalk for a chip exceeds the specification of the critical circuit path on the chip, a circuitry failure will occur. Therefore, it is important to accurately estimate the circuit delay variances for purpose of performance and yield tuning."* (column 1, lines 40-64)].

Chang teaches variables that are related to metallization resistance and metallization capacitance [*"As examples, the thickness, length and width of an interconnect will affect resistance, and the spacing between interconnects will affect capacitance."* (column 1, line 65 – column 2, line 7)].

Chang teaches using a circuit simulator to estimate the performance an integrated circuit based on the metallization resistance and metallization capacitance [*"In a final phase, the randomized RC nets are employed to determine worst-case values for one or both of delay and crosstalk. In the preferred embodiment, a device model is input, enabling estimation of delay and crosstalk for the entire circuit. The 3-sigma delay and crosstalk can be determined from a number of simulations, such as SPICE simulations or a fast delay calculator."* (column 4, lines 26-52)].

Chang discloses numerous equations used to model the performance of the integrated circuit design [(column 6, line 65 – column 15, line 3)].

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to change a circuit design that fails to meet certain predetermined criteria,

such as circuit timing and delay requirements. Teaching and motivation to do so would be found in the knowledge of a person of ordinary skill in the art of integrated circuit design.

Response to Arguments – 35 USC § 103

In response to the rejections above, Applicants argue that:

> In rejecting the claims over Chang, the Examiner incorrectly ignores elements which appear in claims 1 and 37. For example, claim 1 specifically claims providing an equation which comprises a plurality of variables and constants, where the plurality of constants are unknown constants and one of the variables is related to at least one of metallization capacitance and metallization resistance; applying the circuit simulator to a first circuit design to derive a first set of constants for the plurality of constants; replacing the unknown constants with the first set of constants to obtain a performance model of the first circuit design; and performing a first set of timing analyses using the performance model of the first circuit design. These elements clearly appear in the claim and contribute to the method; however they were not specifically addressed in rejected the claims over Chang. The Examiner simply makes broad statements with respect to his claim interpretations.

The Examiner respectfully traverses this argument as follows.

The language of claim 1 renders each of the steps to which Applicants refer futile. The method performs these steps but then completely disregards any and every result that they may have produced by "changing the first circuit design to obtain a second circuit design; and making an integrated circuit comprising the second circuit design."

How can a method be found to be patentable based upon completely irrelevant and futile steps? Would Applicants similarly argue that in another application, were claim 1 to appear with the additional step "count to five," that this meaningless step would define a patently distinct invention? Applicants method provides equations, derives constants, replaces constants, and performs timing analyses for no purpose or result in the claim.

Applicants arguments have been fully considered but have been found unpersuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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